Douglas Jai Fouts, PhD, PE

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Education:

Ph.D. - Electrical and Computer Engineering, University of California, Santa Barbara, California, 1990

EXPERIENCE:

Associate Professor - U.S. Naval Postgraduate School, Department of Electrical and Computer Engineering and Space Systems Academic Group, Monterey, California, July 1996 - present *Teach graduate courses in Electrical and Computer Engineering and Space Systems Engineering: VLSI Design, Advanced VLSI and Mixed-Signal IC Design, Fault Tolerant*

Computing, Microprocessors for Space Applications, Microprocessor Based Systems Design, Computer Architecture, Advanced Computer Architecture and Parallel Processing, Logic Design and Switching Theory, Analog and Digital Circuits, and others. Teach short courses for nondegree students: Digital Signal Processing Hardware for Radar Applications, FPGA Design, etc. Supervise student research, Thesis, and dissertations on topics such as VLSI design, mixed-signal system-on-a-chip design, GaAs and InP digital IC design, the effects of radiation on GaAs and Si digital ICs, high-speed/low-power GaAs and InP logic circuits, fault-tolerant microprocessor systems for space applications, computer architecture, etc.

Assistant Professor - U.S. Naval Postgraduate School, Department of Electrical and Computer Engineering and Space Systems Academic Group, Monterey, California, September 1990 - June 1996

Co-principal Investigator - U.S. Naval Postgraduate School, Department of Electrical and Computer Engineering, October 1, 2002 - September 30, 2005

Contract: Library Development and Experiments Using Prototype Reconfigurable Computing Machines

Sponsor: National Security Agency-*Development of a software library of mathematical functions for crypto logic and signal processing applications for a new type of computer with a reconfigurable architecture. Testing, benchmarking, and evaluation of the new type of computer with a reconfigurable architecture for crypto logic and signal processing applications using the newly developed software library*

Co-principal Investigator - U.S. Naval Postgraduate School, Department of Electrical and Computer Engineering, October 1, 2000 - September 30, 2003

Contract: Digital Target Imaging Architecture For Multiple Large Target Generation

Sponsor: Office of Naval Research and Naval Research Laboratory - *Development of equations and algorithms necessary to digitally synthesize false radar return images in electronic attack systems to counter wideband imaging radars. Development of a system-level architecture, a micro architecture, and a system-on-a-chip implementation for use in the U.S. Navy Advanced Integrated Electronic Warfare System.*

Principal Investigator - U.S. Naval Postgraduate School, Space Systems Academic Group

and Department of Electrical and Computer Engineering, Monterey, California, May 1999 - April 2000

Contract: CEPXS/SPICE Automated Software Interface Development

Sponsor: Lockheed Martin Space and Missile Systems - *Development of an automated software interface between CEPXS (Coupled Electron/Proton Transport Simulator) and SPICE (Simulation Program with Integrated Circuit Emphasis) to allow accurate simulation of the operation of microelectronic circuits while exposed to nuclear radiation.*

Co-principal Investigator - U.S. Naval Postgraduate School, Space Systems Academic Group and Department of Electrical and Computer Engineering, Monterey, California, October 1995 - September 1998

Contract: Radiation-Immune, High-Speed, Low-Power, Gallium Arsenide, Digital Integrated Circuits

Sponsor: National Security Agency/U.S. Navy - Space and Naval Warfare Systems Command/U.S. Naval Research Laboratory-*Theoretical and laboratory investigation of the effects of buried, low temperature grown, buffer layers on the single event upset sensitivity of gallium arsenide integrated circuits. Development of high-speed, low-power, radiation-immune, GaAs ICs using substrates with buried, low-temperature grown, buffer layers.*

Principal Investigator - U.S. Naval Postgraduate School, Space Systems Academic Group and Department of Electrical and Computer Engineering, Monterey, California, October 1996 - September 1998

Contract: Radiation Tolerant Bulk CMOS Digital Integrated Circuits

Sponsor: National Security Agency - *Experimental investigation of circuit and mask layout techniques for producing radiation-tolerant digital ICs using commercial bulk CMOS fabrication processes.*

Principal Investigator - U.S. Naval Postgraduate School, Department of Electrical and Computer Engineering, Monterey, California, October 1997 - September 1998

Contract: Tactor Interface and Controller Design for the Tactile Situational Awareness System

Sponsor: Naval Aerospace Medical Research Laboratory - *Development of a single-chip VLSI tactor interface and microcontroller for interfacing to and controlling a tactile situational awareness system.*

Principal Investigator - U.S. Naval Postgraduate School, Department of Electrical and Computer Engineering, Monterey, California, October 1996 - September 1997

Contract: Dynamic Logic Circuits for Complimentary GaAs Fabrication Processes

Sponsor: National Security Agency - *Simulation and experimental investigation of low-power, high-speed, dynamic logic circuits for use with complementary GaAs fabrication processes.*

Principal Investigator - U.S. Naval Postgraduate School, Department of Electrical and Computer Engineering, Monterey, California, October 1995 - September 1997

Contract: Read Prediction Cache Memories for Embedded Microprocessor Systems

Sponsor: U.S. Navy - Space and Naval Warfare Systems Command - *Theoretical and simulation investigation of data cache miss address prediction methods. Development of alternatives to off-chip, second-level, cache memories for spacecraft, weapon system, and other embedded high-performance microprocessor applications.*

Principal Investigator - U.S. Naval Postgraduate School, Space Systems Academic Group and Department of Electrical and Computer Engineering, Monterey, California, October 1995 - September 1996

Contract: Evaluation of CAD/CAM Software Tools for Designing Radiation-Hardened Digital Integrated Circuits

Sponsor: National Security Agency - *Investigation and evaluation of commercial CAD/CAM software tools for use in designing space qualified digital integrated circuits using a proprietary radiation-hardened cell library.*

Principal Investigator - U.S. Naval Postgraduate School, Space Systems Academic Group and Department of Electrical and Computer Engineering, Monterey, California, October 1992 - September 1995

Contract: Radiation Tolerant, High-Speed, Low-Power, Gallium Arsenide Dynamic Logic

Sponsor: U.S. Navy - Space and Naval Warfare Systems Command - *Laboratory investigation of single event upsets caused by ionizing radiation in gallium arsenide dynamic logic circuits. Development of new circuits and techniques for use in radiation-tolerant, high-speed, low-power computers and digital systems.*

Principal Investigator - U.S. Naval Postgraduate School, Department of Electrical and Computer Engineering, Monterey, California, October 1990 - September 2002

Contract: VLSI Design Education

Sponsor: National Science Foundation/MOSIS Educational Program - *Received funding for fabricating integrated circuits designed by students in the VLSI design courses that I teach.*

Principal Investigator U.S. Naval Postgraduate School, Department of Electrical and Computer Engineering, Monterey, California, October 1990 - September 1992

Contract: Design Principles for Very High-Speed Digital Circuits and Systems

Sponsor: U.S. Naval Postgraduate School, Research Initiation Program - *Initiated a new research program in gallium arsenide (GaAs) digital IC design. Research focused on the design of new, high-speed driver, receiver, and transceiver circuits for bus-connected digital systems and computers.*

Research Assistant - University of California, Department of Electrical and Computer Engineering, Santa Barbara, California, June 1985 - June 1990

Contract: Gallium Arsenide Design Principles

Sponsor: Defense Advanced Research Projects Agency

Principal Investigators: Dr. Stephen I. Long and Dr. Steven E. Butner - *Participated in the design and construction of a functional IC tester for testing GaAs digital ICs at speeds up to 1 GHz. Responsible for the overall architecture of the tester and the design and implementation of a custom GaAs IC used in its construction. Designed, probed, and characterized numerous GaAs test structures. Conducted a study of packaging and interconnection techniques for high speed GaAs logic. Assisted in the development of a graduate level course in GaAs digital IC design. Assisted in teaching DARPA sponsored course on teaching GaAs digital IC design.*

Associate Engineer - Burroughs Corporation (now UNISYS), Computer Systems Group, Mission Viejo, California, September 1980 - January 1983 *-Participated in the design and debugging of a new, large systems, main frame computer utilizing advanced technologies and design methodologies. Responsible for debugging the I/O processor, including the development of diagnostic and maintenance software.*

Visiting Lecturer - University of California, Department of Electrical and Computer Engineering, Santa Barbara, California, September 1986 - December 1986- *Taught upper division undergraduate course on computer architecture.*

Instructor University of California Extension Service, Santa Barbara, California, August 1985 - *Taught high-speed packaging and interconnect section of industry-oriented UC extension course on high speed gallium arsenide ICs.*

Student - The Aerospace Corp., Space Computers Laboratory, El Segundo, California, June 1979 - September 1979 *Designed, constructed, and debugged hardware to interface an I/O subsystem to a satellite-based microcomputer system.*

REGISTRATION: Registered professional engineer, state of California, branch of Electrical Engineering, number E 16158.

EDUCATION: Ph.D. University of California, Santa Barbara, California, Electrical and Computer Engineering, July 1990

Area of Specialization: Computer Engineering

Minor Areas: Analog and Digital Circuits, Computer Science, Applied Mathematics

Course work and research *emphasized the study of high-performance digital logic circuits and computer architecture with special emphasis on the design and implementation of high-speed gallium arsenide digital integrated circuits and systems. Silicon VLSI and compiler issues related to high-performance computer architectures were also studied.*

M.S. University of California, Santa Barbara, California, Electrical and Computer Engineering, December 1984

Area of Specialization: Computer Engineering

Minor Areas: VLSI, Computer Science

Course work and research *emphasized the study of digital IC design, computer architecture, digital systems design, compilers, and operating systems, with special emphasis on high speed numeric processing.*

B.A. University of California, Berkeley, California, Computer Science, August 1980

Areas of Study: Computer Architecture, Logic Design, Compilers, Operating Systems

PATENTS :

D.J. Fouts, P.E. Pace, "Single-Chip False Target Radar Image Generator for Countering Wideband Imaging Radars", Patent Pending, Navy Case #83887.

D.J. Fouts and K.A. Shehata, "Two-Phase Dynamic Logic Circuits for Gallium Arsenide Complementary HIGFET Fabrication Processes", U.S. Patent No. 6,150,848, November 21, 2000.

D.J. Fouts, "Predictive Read Cache Memories for Reducing Primary Cache Miss Latency in Embedded Microprocessor Systems", U.S. Patent No. 6,047,359, April 4, 2000.

D.J. Fouts and K.A. Shehata, "Two-Phase Dynamic Logic Circuits for Gallium Arsenide Complementary HIGFET Fabrication Processes", U.S. Patent No. 5,926,038, July 20, 1999.

PUBLICATIONS:

P.E. Pace, D.J. Fouts, S. Ekestorm, and C. Karow, "A Digital False-Target Image Synthesizer for Countering ISAR", *Proceedings of the IEEE* accepted for publication.

D.J. Fouts, P.E. Pace, C. Karow, and S. Ekestorm, "A Single-Chip False Target Radar Image Generator for Countering Wideband Imaging Radars", *IEEE Journal of Solid State Circuits*, Vol. 37, No. 6, Jun. 2002, pp. 751-759.

D.J. Fouts, G.R. McKerrow, G.K. Lum, S.S. Noe, and A.S. Lambley, "Second-Layer Polysilicon Structures for Gate End-Around Leakage Current Compensation in Bulk CMOS ICs", *Microelectronics Reliability,* Vol. 40, No. 6, Jun. 2000, pp. 955-963.

D.J. Fouts and T.R. Weatherford, "Gallium Arsenide Field Effect Transistor Logic Circuits", The Wiley Encyclopedia of Electrical and Electronics Engineering, Volume 8, John G. Webster, Editor, John Wiley and Sons, New York, NY, 1999, pp. 215-233.

D.J. Fouts, G.J. Nowicki, M.E. Aguilar, "A CMOS Read Prediction Buffer IC for Embedded Microprocessor Systems", *Journal of Microelectronic Systems Integration*, Vol. 5, No. 3, Sep.1997, pp. 129-138.

T.R. Weatherford, R. Radice, D. Eskins, J. Devers, D.J. Fouts, P.W. Marshall, C.J. Marshall, H. Dietrich, M. Twigg, and R. Milano, "SEU Design Considerations for MESFETs on LT GaAs", *IEEE Transactions on Nuclear Science*, Vol. 44, No. 6, Dec. 1997, pp. 2282-2289.

T.R. Weatherford, P.W. Marshall, C.J. Marshall, D.J. Fouts, B. Mathes, and M LaMacchia, "Effect of Low-Temperature Buffer-Layer Thickness and Growth Temperature on the SEE Sensitivity of GaAs HIGFET Circuits", *IEEE Transactions on Nuclear Science*, Vol. 44, No. 6, Dec. 1997, pp. 2298-2305.

D.J. Fouts, T.R. Weatherford, D. McMorrow, K. Wolfe, S.E. Van Dyk, and A.B. Campbell, "Single Event Upsets in Gallium Arsenide Pseudo-Complementary MESFET Logic" *IEEE Transactions on Nuclear Science*, Vol. 42, No. 6, Dec. 1995, pp. 1829-1839.

D.J. Fouts, T.R. Weatherford, D. McMorrow, J.S. Melinger, and A.B. Campbell, "Single Event Upsets in Gallium Arsenide Dynamic Logic" *IEEE Transactions on Nuclear Science*, Vol. 41, No. 6, Dec. 1994, pp. 2244-2251.

D.J. Fouts and A.B. Billingsley, "Predictive Read Caches: An Alternative to On-Chip Second-Level Cache Memories" *Journal of Microelectronic Systems Integration*, Vol. 2, No.2, Jun. 1994, pp. 109-121.

D.J. Fouts, "A Gallium-Arsenide Digital Phase Shifter for Clock and Control Signal Distribution in High-Speed Digital Systems", *IEEE Journal of Solid State Circuits*, Vol. 27, No. 5, May 1992, pp. 802-809.

D.J. Fouts and S.E. Butner, "Architecture and Design of a 500MHz Gallium Arsenide Processing

Element for a Parallel Super Computer", *IEEE Journal of Solid State Circuits, Second Special Issue on Microelectronic Systems*, Vol. 26, No. 9, Sep. 1991, pp. 1199-1211.

D.J. Fouts, J.M. Johnson, S.E. Butner, and S.I. Long, "System Architecture of a 1 GHz Digital IC Tester", *IEEE Computer*, Vol. 20, No. 5, May 1987, pp. 58-70. **Reprinted in two IEEE tutorials.**

D.J. Fouts, P.E. Pace, C. Karow, S. Ekestorm, "A Digital ASIC for Synthesizing False Target Radar Images", *Asilomar Conference on Signals, Systems, and Computers*, Pacific Grove, CA, Nov. 3-6, 2002.

J.P. Link and D.J. Fouts, "A Bus Interface Chip for Tactile Communications", *Government Microcircuit Applications Conference*, Monterey, CA, pp. 460-463, Mar. 1999.

D.J. Fouts, K.A. Shehata, and S. Michael, "Dynamic Logic Families for Complementary Gallium Arsenide (CGaAs) Fabrication Processes", *40th IEEE Midwest Symposium on Circuits and Systems*, Sacramento, CA, Aug. 1997.

K.A. Shehata, D.J. Fouts, and S. Michael, "A Dynamic Fout-Bit Carry Lookahead Adder Circuit for Complementary Gallium Arsenide (CGaAs) Fabrication Processes", *40th IEEE Midwest Symposium on Circuits and Systems*, Sacramento, CA, Aug. 1997.

T.R. Weatherford, D.J. Fouts, P.W. Marshall, C.J. Marshall, and H.D. Dietrich, "Soft Error Immune GaAs Circuit Technologies", *40th IEEE Midwest Symposium on Circuits and Systems*, Sacramento, CA, Aug. 1997.

R.J. Barton III, T.O. Walker III, and D.J. Fouts, "A CMOS Current-Mode Full-Adder Cell for Multi-Valued Logic VLSI", *40th IEEE Midwest Symposium on Circuits and Systems*, Sacramento, CA, Aug. 1997.

T.R. Weatherford, P.W. Marshall, C.J. Marshall, D.J. Fouts, B. Mathes, and M. LaMacchia, "Effects of Low Temperature Buffer Layer Thickness and Growth Temperature on the SEE Sensitivity of GaAs HIGFET Circuits", *34th Annual International Nuclear and Space Radiation Effects Conference*, Snowmass Village, CO, Jul. 1997.

T.R. Weatherford, R. Radice, D. Eskins, J. Devers, D.J. Fouts, P.W. Marshall, C.J. Marshall, H. Dietrich, M. Twigg, and R. Millano, "SEU Design Consideration for MESFETs on LT GaAs", *34th Annual International Nuclear and Space Radiation Effects Conference*, Snowmass Village, CO, Jul. 1997.

E. Ledbetter, T.R. Weatherford, G. David, J. Hayden, J. Whitaker, and D.J. Fouts, "In Situ Picosecond Resolution Measurements of Charge Collection Transients in GaAs Logic", *34th Annual International Nuclear and Space Radiation Effects Conference*, Snowmass Village, CO,

Jul. 1997.

Meritorious Paper Award: D.J. Fouts, T.R. Weatherford, C.J. Dale, P.W. Marshall, H.B. Dietrich, D. McMorrow, J. Abrokwah, M. LaMacchia, and R. Milano, "Soft-Error Immune Gallium Arsenide ICs Using COTS Designs and Foundries", *Government Microcircuit Applications Conference*, Mar. 10-13 1997, Las Vegas, NV.

T.J. Gallander and D.J. Fouts, "Design Tradeoffs in Radiation Hardened ASICs for Space Applications" *Government Microcircuit Applications Conference*, Mar. 10-13 1997, Las Vegas, NV.

Invited Paper: D.J. Fouts, T.R. Weatherford, P.W. Marshall, C.J. Marshall, H.B. Dietrich, M. Twigg, M. LaMacchia, J. Abrokwah, and R. Milano, "Low-Temperature Gallium Arsenide Soft-Error Immune Digital Integrated Circuits", *1997 Radiation Environmental Effects Forum*, Chantilly, VA, Feb. 1997.

G. David, J.F. Whitaker, E.J. Ledbetter, T.R. Weatherford, D. Fouts, W. Goyette, K. Jobe, and K. Elliott, "A Picosecond-Response Photoconductive-Sampling Probe for Digital Circuit Testing", *Proceedings of the 1996 Lasers and Electro-Optics Conference*, San Francisco, CA, pp. 236-237, Nov. 1996.

D.J. Fouts, T.R. Weatherford, D. McMorrow, K. Wolfe, S.E. Van Dyk, and A.B. Campbell, "Single Event Upsets in Gallium Arsenide Pseudo-Complementary MESFET Logic" *32nd Annual International Nuclear and Space Radiation Effects Conference*, Madison, WI, Jul. 1995.

D.J. Fouts, T. Weatherford, D. McMorrow, J.S. Melinger, and A.B. Campbell, "Single Event Upsets in Gallium Arsenide Dynamic Logic", *31st Annual International Nuclear and Space Radiation Effects Conference*, Tucson, AZ, Jul. 1994.

J.K. Richstein, D.J. Fouts, and R.J. Pieper, "A CMOS VLSI IC For Real-Time Opto-Electronic Two-Dimensional Histogram Generation", *Twenty-Sixth IEEE Southeastern Symposium on System Theory*, Athens, OH, Mar. 1994.

D.J. Fouts and T.C. Gonter, "A Microprocessor Interface for Ferroelectric Capacitor Memory", *Twenty-Sixth Annual IEEE Asilomar Conference on Signals, Systems, and Computers*, Pacific Grove, CA, Oct. 1992.

A. Billingsley, D.J. Fouts, and R. Hamming, "Memory Latency Reduction Using an Address Prediction Buffer", *Twenty-Sixth Annual IEEE Asilomar Conference on Signals, Systems, and Computers*, Pacific Grove, CA, Oct. 1992.

D.J. Fouts, "A Phasing Adjustment and Fanout Buffer For Distributing Clock and Control Signals

in High-Speed Digital Systems", *IEEE Thirty-Fourth Midwest Symposium on Circuits and Systems*, Monterey, CA, May 1991.

Invited Paper: D.J. Fouts, J.M. Johnson, S.E. Butner, and S.I. Long, "System Architecture of a GaAs 1 GHz Digital IC Tester", *Twentieth IEEE Hawaii International Conference on System Sciences*, Kona, HI, Jan. 1987.

D.J. Fouts, *Theory, Design, and Simulation of GASP: A Block Data Flow Architecture for Gallium Arsenide Super Computers*, Ph.D. Dissertation, Univ. of Calif., Santa Barbara, CA, Jul. 1990.

D.J. Fouts, *A High Performance Peripheral Array Processor for Engineering Work Stations*, M.S. Thesis, Univ. of Calif., Santa Barbara, CA, Sep. 1984.

D.J. Fouts, "Collinear Phased Arrays for HF Communication", *QST*, Vol. 73, No. 3, pp. 29-32, Mar. 1989.

AWARDS and RECOGNITIONS

Winner of the 2002 Menneken Award for Excellence in Scientific Research.

Received 1997 Outstanding Research Achievement award for the Department of Electrical and Computer Engineering, U.S. Naval Postgraduate School, Monterey, CA.

Received 1996 Outstanding Instructional Performance award for the Space Systems Academic Group, U.S. Naval Postgraduate School, Monterey, CA.

Granted academic tenure by the U.S. Naval Postgraduate School, Monterey, CA, July 1996.

Received 1993 Outstanding Research Achievement award for the Space Systems Academic

Group, U.S. Naval Postgraduate School, Monterey, CA.

AFFILIATIONS

Institute of Electrical and Electronics Engineers, IEEE Computer Society, IEEE Circuits and Systems Society, American Radio Relay League

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Last modified on 17 March 2003